REMARKS

Claims 1-14 are pending.

Claims 1-7 and 11 have been amended to correct informalities, dependencies and to correct antecedent basis problems.

Claims 15 has been added to capture allowable material in Claim 4 with limitations of Claim 1 from which it depends. New Claim 16 depends from Claim 15 and contains the limitations of Claim 5. New Claim 17 depends from Claim 16 and contains the limitations of Claim 6.

Claim 2 has been rewritten independent form including the limitations of Claim 1 from which it depends to capture allowable material. Claims 4-5 have been amended to correctly depend from Claim 2.

Original claims 2-4 where are allowed. The Applicants thanks the Examiner for allowing these claims.

The Applicants respectfully assert that the amendments to Claim 1, 6-7, and 11 and incorporated by reference in any claims depending therefrom, are not narrowing amendments made for a reason related to the statutory requirements for a patent that will give rise to prosecution history estoppel. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831, 1839-40, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 234 F.3d 555, 566, 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2001).

I. REJECTION UNDER 35 U.S.C. § 112

The Examiner rejected Claims 8-10, 12 and 14 under *35 U.S.C. § 112*, first paragraph as failing to comply with the written description requirement. Specifically the Examiner asserts that the claim(s) contains subject matter which is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The Examiner states, with respect to Claim 8, that the limitation "setting said first termination voltage at an optimized level corresponding to said quality of said data signal" has not been taught in the specification. The Applicants refer the Examiner to page 21, lines 11-15 of the Specification. "A test mode may be employed where known data signals are transmitted and received and the termination voltage is adjusted while monitoring the states of the received signals on the output of the receivers. In this manner, the system may be optimized or tested for noise margin in an actual operation environment without resorting to probing methods." The Applicants respectfully assert that they believe adjusting the terminating voltage is the same as setting and it is clear that the terminating voltage is adjusted so the system may be optimized for noise margin which is a quality of the received data signals.

The Applicants also refer the Examiner to page 3, lines 20-22 wherein it is stated "the data termination networks have programmable resistor dividers that allow the termination voltage to be varied under system control to optimize noise margins or to test the signal transmission network."

Therefore, the Applicants assert that the rejection of Claim 8 under *35 U.S.C. § 112* is traversed by the above arguments.

Claims 9 and 10 depend from Claim 8. The Examiner did not specifically detail his rejections of these claims under *35 U.S.C. § 112*, therefore the Applicants assumes they are rejected because base Claim 8 is rejected. Therefore, the Applicants assert that the rejections of Claims 9 and 10 under *35 U.S.C. § 112* are traversed for the same reasons as Claim 8.

The Examiner states, with respect to Claims 12 and 14, that the limitation "circuitry for coupling said second output and said third output to said reference voltage, wherein said reference voltage is modulated by a selected frequency content of said clock signal and said complement clock signal" has not been taught in the specification. Claim 12 recites "circuitry for transmitting said clock signal on a second transmission line, circuitry for transmitting a complement of said clock signal on a third transmission, and

circuitry for terminating said clock signal at a second output of said second transmission line, and circuitry for terminating said complement clock signal at a third output of said third transmission line." The Examiner states that the Specification only teaches the outputs of TN 123 and 124 are coupled to a filter network FN 125 which generates reference output 110. The Applicants refer the Examiner to FIG. 2 wherein clock signal (CLK 209) is transmitted on transmission line 214 (second transmission line). Circuitry 219 is the circuitry for terminating the clock signal (CLK 209) at a second output (233). Circuitry 220 is the circuitry for terminating the complementary clock signal (CLK_N 210) at a third output (234). Resistor 221 is the circuitry for coupling said second output (233) and resistor 222 is the circuitry for coupling said third output (234) to said reference voltage (VREF 226), wherein said reference voltage (VREF 226) is modulated by a selected frequency content (determined by the low pass filtering of capacitor 227) of said clock signal (CLK 209) and said complement clock signal (CLK 210). The Specification on page 8, lines 17-26 and page 9, lines 1-13 discuss in detail the operation of this circuitry. Further discussion of the operation of the circuitry is found in the Specification, page 8, lines 8-16.

Further more Claims 12 and 14 are fully supported by FIG. 1, FIG. 2 and the description of these figures.

The Applicant, therefore, respectfully asserts that the rejections of Claims 12 and 14 under *35 U.S.C. §* 112 as failing to comply with the written description requirement are traversed by the above arguments.

The Applicants have amended Claim 6 to read "said N resistor voltage divider networks....." to correct the antecedent basis problem pointed out by the Examiner. The Applicant, therefore, respectfully asserts that the rejection of Claims 6 under *35 U.S.C. §* 112 as having insufficient antecedent basis is traversed by the amendment to Claim 6.

The Applicants have amended Claim 11 to remove "said I/O adapter", which was inadvertently included, to correct the antecedent basis problem pointed out by the Examiner. The Applicant, therefore, respectfully asserts that the rejection of Claims 11

and 12 under *35 U.S.C. § 112* as having insufficient antecedent basis is traversed by the amendment to Claim 11.

II. REJECTION UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 1, 5, and 13 under *35 U.S.C. § 103(a)* as being unpatentable over U.S. Patent No. 6,105,157 to *Miller* (hereafter "*Miller*") in view of U.S. Patent No. 3,993,867 to *Blood* (hereafter "*Blood*").

The Examiner rejected Claim 7 under *35 U.S.C. § 103(a)* as being unpatentable over *Miller* in view of *Blood* and further in view of U.S. Patent 5, 761,246 to *Cao et al.* hereafter ("*Cao*") and U.S. Patent 6,442,644 to *Gustavson et al.* hereafter ("*Gustavson*").

To establish a *prima facie* case of obviousness, the Examiner must meet three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be some reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations.

The Examiner states that *Miller* discloses a digital transmission system comprising the limitations of Claim 1. *Miller* fails to teach a first receiver input coupled to a first output of said first transmission line and a second receiver input coupled to a reference voltage as recited in Claim 1. *Miller* also fails to teach a first terminating network receiving programming signals and generating a first terminating voltage with a first source impedance at a first node, wherein the first node coupled to the first output of the first transmission line and the first terminating voltage is modified in response to said programming signals while maintaining a magnitude of said first source impedance.

In Claim 1 of the present invention, the first node is coupled to the first output of the transmission line, the first input of the first receiver circuit, and to the first terminating network that receives programming signals and generates a first termination voltage with a first source impedance at the first node. The Examiner states that node 20

is the first node. Node 20 is connected to the DUT (device under test). There is no first terminating network coupled to node 20 in FIG. 1 of *Miller*. Programmable impedances 24A and 24B are coupled to the input of transmission line 16A and the output of transmission line 16B and neither generate a first termination voltage with a first source impedance nor connect to node 20 (input of receiver circuit). Further, by the Examiner's own admission, *Miller* does not disclose that the first receiver circuit has a second receiver input coupled to a reference voltage.

The Examiner also states that *Miller* does not disclose the first node coupled to the output of the first transmission line. The Applicants further assert that *Miller* also does not teach or suggest that the first terminating voltage is modified in response to the programming signals while maintaining a magnitude of the first source impedance.

The system of *Miller* is for calibrating tester channels. The tester sends a test signal to a DUT 12 on exemplary transmission line 16A. The test signal is sampled by the DUT 12 at node 20. The test signal propagates to resistive terminator 24B which prevents any reflections if sized correctly. After the test signal is sent by driver 26, it is put into tri-state mode so as not to interact with any response signal sent by the DUT in response to its sampled test signal. DUT 12 responds to the test signal by sending a response signal. This response signal travels down both transmission lines 16A and 16B. Driver 26 is in tri-state mode, therefore, the response signal is adsorbed by resistor terminator 24A with no reflections as there is not receiving circuit to sample the signal at driver 26. The response signal only needs to travel down transmission line 16B to compare circuit 30 where it is compared with the expected value from the compare signal from circuit 28. Resistor terminator 24B, if sized correctly prevent reflections from traveling back transmission line 16B to DUT 12.

In summary, *Miller* does not disclose sending a drive signal down a first transmission line whose output is terminated in a termination network coupled to the input of a receiver, wherein the termination network sets a termination voltage level in response to programming signals while maintaining a pre-determined source impedance as recited by Claim 1. Further the *Miller* does not disclose that the receiver has a second

input coupled to a reference voltage. Therefore, the Applicants respectfully assert that the *Miller* does not teach or suggest the invention of Claim 1.

The Examiner, however, states that *Blood* teaches a second receiver input coupled to a reference voltage and cites FIG 2 and 4, element Y, and column 2, lines 53-68, column 3, lines 58-68, and column 6, lines 3-24. Element Y is the output of a current switch S2 that generates a logic replica of the signal being transmitted by S1 and is coupled to the input of element DA which is a voltage comparator and is not a receiver. See *Blood*, column 3, line 66. Comparator DA is used to compare the composite signal at X with the logic replica of the signal being transmitted by S1 to separate the full duplex signals on line 11. *Blood* does not teach or suggest the second receiver coupled to a reference voltage as recited in Claim 1 of the present invention.

Blood discloses a full duplex signaling system wherein the resistors RL and RL' are used to sum the transmitted and received currents from transmitters T1 and T2. Comparator DA with the replica of the input signal at input X is used to separate the signal transmitted from transmitter T1 from the composite signal across RL. The driver S1 of *Blood* coupled to the input of transmission line 11 is a current source which cannot be substituted for the driver of *Miller* which is a voltage source driver.

The transmission system of *Blood* has simultaneous driving and receiving at each end of transmission line 11 (at RL and RL'). For RL and RL' to work as terminators for the characteristic impedance of the lines, the receiver and the driver (current source S1) both must have a high source impedance so that the voltage that signals from station A arriving at RL' "see" only the impedance of RL' which is in parallel with the impedance of the comparator DA' and the driver (current switch S1') at RL'. Likewise signals from station B, which may arrive simultaneous (full duplex) with drive signals at RL "see" only the impedance of RL which is in parallel with the impedance of the driver (current switch S1) and comparator DA at RL.

In view of the above, one of ordinary skill in the art clearly would see that the system of *Miller* and the system of *Blood* do not allow their drivers and receivers to be

interchanged. Therefore the teachings of *Miller* and *Blood* cannot be combined to arrive at the invention of Claim 1.

The Applicants have shown that the system of *Miller* does not disclose the invention of Claim 1. *Blood* discloses a full duplex system that employs current source drivers and receivers at both ends of a transmission line with termination resistors at both ends of the transmission lines which are fixed. *Blood* does not teach or suggest a termination network coupled to the input of the receiver that generates a termination voltage with a source impedance, wherein the termination voltage is modified in response to programming signals while maintaining a magnitude of the source impedance.

The Applicants have shown and the Examiner admits that *Miller* does not teach or suggest the invention of Claim 1. The Applicants have shown that *Blood* does not teach or suggest those limitations of Claim 1 that the Examiner admits are not taught or suggested by *Miller*, rather *Blood* discloses a means for separating a transmitted signal from a received composite, transmitted and received, full duplex signal. The Applicants assert that neither *Miller* nor *Blood*, singly or in combination, teach or suggest the invention of Claim 1. Therefore, the Applicants respectfully assert that the rejection of Claim 1 under *35 U.S.C. § 103(a)* as being unpatentable over *Miller* in view of *Blood* is traversed by the above arguments.

Claim 5 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 5 adds the limitation that the first terminating voltage is modified in a number M integer increments. The Examiner rejected Claim 5 by stating that by considering M to equal to one then all the limitations are the same as Claim 1.

The Applicants have shown that neither *Miller* or *Blood* teach or suggest a termination network that generates a termination voltage with a source impedance, wherein the termination voltage is modified in response to programming signals. Considering M only equal to one is to imply the termination voltage is not modified or varied. Claim 5 is directed to how the termination voltage of Claim 1 is modified (a number M integer increments). Since neither *Miller* or *Blood*, singly or in combination,

teach or suggest a termination network that generates any termination voltage, they do not address how that termination voltage is modified in response to programming signals.

Therefore, the Applicants respectfully assert that the rejection of Claim 5 under *35 U.S.C. § 103(a)* as being unpatentable over *Miller* in view of *Blood* is traversed by the above arguments and for the same reason as Claim 1.

Claim 13 is an independent claim directed to a signal transmission system. The Examiner rejects Claim 13 for the same reasons as Claim 1. The Applicants assert that the Examiner failed to make a *prima facie* case of obviousness for failing to specifically address the limitations of independent Claim 13. Therefore, the Applicants respectfully assert that the rejection of Claim 13 under *35 U.S.C. § 103(a)* as being unpatentable over *Miller* in view of *Blood* is traversed by the above arguments and for the same reason as Claim 1.

Claim 7 has been amended to correct an informality and to clearly indicate the reference voltage is generating from the first and second clock. Claim 7 is directed to a digital signal transmission system that is disposed in first and second ICs. The first IC has a driver circuit receiving a data signal and generating a data signal output, said data signal output coupled to a first input of a first transmission line. The second IC has a termination network receiving programming signals and generating a termination voltage having a first source impedance in response to the programming signals at a termination node, wherein the termination node is coupled to an output of the first transmission line. The second IC also has a differential receiver in having a second input coupled to the termination node and a third input coupled to a reference voltage and a reference network receiving a first clock transmitted from the first IC with a second transmission line, a second clock transmitted from the first IC with a third transmission line, the programming signals, and generating the reference voltage in response to the first and second clock, wherein the terminating voltage is varied in response to the programming signals while maintaining a pre-determined magnitude of the first source impedance.

The Examiner states that the combination of *Miller* and *Blood* teach all the limitations of Claim 7 except they do not teach that the driver, termination network, and a differential receiver can be implemented in an integrated circuit (IC) and they do not teach a reference network receiving a first clock transmitted from the first IC with a second transmission line, a second clock transmitted from the first IC with a third transmission line. The Examiner fails to state that *Miller* and *Blood* also do not teach that the second IC has a termination network receiving programming signals and generating a termination voltage having a first source impedance in response to the programming signals at a termination node network and generates the reference voltage in response to the first and second clock. The Examiner has failed to make a *prima facie* case that *Miller* and *Blood* teach all the limitations of Claim 7 except those noted since the Examiner has not addressed all the limitations of Claim 7 including the specific claim language which describes the elements of Claim 7 and their relationships.

The Examiner does not state that *Cao* teaches all the limitation of Claim 7, rather the Examiner states that *Cao* teaches that the driver is implemented in the first chip and the differential receiver is implemented in the second chip and it is inherent that the programmable resistive network can be implemented within chip 2 or integrated circuit 2, IC 2. The Applicants respectfully assert that *Cao* does not show any termination network in FIG. 1 cited by the Examiner. *Cao* only shows communication between two ICs using a scheme where *Cao* claims multiple digital signals may be sent simultaneously on a single transmission line. *Cao* shows no termination network of the transmission line in FIG. 1 nor does *Cao* show any programming signals received by a termination network. The Examiner only shows that *Cao* has a driver in a first IC and a receiver in a second IC. Examiner has not shown where *Cao* adds anything to the teachings of *Blood* and *Miller* that would lead anyone of ordinary skill in the art to the invention of Claim 7.

The Examiner states that *Miller*, *Blood* and *Cao* fail to teach a reference network receiving, a first clock transmitted from the first IC with a second transmission line, a second clock transmitted from the first IC with a third transmission line, the programming signals, and generating the reference voltage in response to the first and

second clock as recited in amended Claim 7. The Examiner, however, states that *Gustavson* teaches that a reference network (150) receives a first clock (DCLK_1B) over a second transmission line (156b) and a second clock (DCLK_1B*) over a third transmission line (156c). Element 150 in FIG. 1A is a command module 150. The Applicants do not see the relevance of *Gustavson* since nowhere does *Gustavson* teach or suggest that command module 150 generates a reference voltage in response to the first and second clock, wherein the reference voltage is coupled to the third input of the differential receiver that receives the data signal over the first transmission line at its second input as recited in Claim 7. The fact that *Gustavson* sends two clock signals each over a transmission line in a data link, does not read of the limitations of Claim 7.

The Examiner has stated that neither *Miller*, *Blood*, and *Cao*, singly or in combination teach or suggest all the elements of the invention of Claim 7. The Examiner has not shown that *Gustavson* adds any relevant teachings relative to Claim 7. The Examiner has only shown that *Gustavson* transmits two clocks over separate transmission lines on a data link without showing where *Gustavson* teaches any of the limitations of Claim 7 that he admits *Miller*, *Blood*, and *Cao*, singly or in combination do not teach or suggest. Therefore, the Applicants respectfully assert that the rejection of Claim 7 under *35 U.S.C. § 103(a)* as being unpatentable over *Miller* in view of *Blood* and further in view of *Cao* and further in view of *Gustavson* is traversed by the above arguments.

III. CONCLUSION

The rejection of Claims 8-10, 12 and 14 under *35 U.S.C. § 112*, second paragraph as failing to comply with the written description requirement have been traversed.

The rejection of Claims 6, 11, and 12 under *35 U.S.C. § 112*, first paragraph as failing to point out and distinctly claim the subject matter the Applicants regard as his invention have been traversed.

The rejections of Claims 1, 5, and 13 under *35 U.S.C. § 103(a)* as being unpatentable over *Miller* in view of *Blood* has been traversed.

The rejection of Claim 7 under *35 U.S.C. § 103(a)* as being unpatentable over *Miller* in view of *Blood*, further in view of *Cao* and further in view of *Gustavson* has been traversed.

Claims 2 has been rewritten in independent form including the limitations of Claim 1 to capture allowable material.

Claims 15, 16, and 17 have been added to capture allowable material in Claim 4.

The Applicants, therefore, respectfully assert that amended Claims 1-7 and 11, Claims 8-10, Claims 12-14 and new Claims 15-17 are now in condition for allowance and request an early allowance of these claims.

Applicants respectfully request that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Patent Agent and Attorney for Applicants

By: Richard F. Frankeny

Richard F. Frankeny
Reg. No. 47,573
Kelly K. Kordzik
Reg. No. 36,571

P.O. Box 50784
Dallas, Texas 75201
(512) 370-2872

Austin_1 281984v.1